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APPLICANTS

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** CONTINUING DATA *****

THIS APPLICATION IS A 371 OF PCT/JP00/06824 09/29/2000

Yes 1ms

** FOREIGN APPLICATIONS *****

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Yes 1ms

IF REQUIRED, FOREIGN FILING LICENSE GRANTED

** 12/28/2001

Foreign Priority claimed	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no	STATE OR COUNTRY JAPAN	SHEETS DRAWING 7	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
35 USC 119 (a-d) conditions met	<input checked="" type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after Allowance				
Verified and Acknowledged	<i>John S. Berridge</i> Examiner's Signature	<i>IMS</i> Initials			

ADDRESS

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TITLE

Interconnect substrate, semiconductor device, methods of fabricating, inspecting, and mounting the semiconductor device, circuit board, and electronic instrument

FILING FEE RECEIVED 860	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:	<input type="checkbox"/> All Fees
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